Notice of Allowability	Application No.	Applicant(s)	
	09/841,569	ECKELMAN ET AL.	
	Examiner	Art Unit	
	Mujtaba K. Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *12/8/2005*.

2. ☒ The allowed claim(s) is/are *1-7*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

REASONS FOR ALLOWANCE

Claims 1-7 are allowed. The following is an Examiner's statement of reasons for allowance:

Independent claim 1 of the present application teaches a method for real time capture of desired failing chip cell diagnostic information from high speed testing of a semiconductor chip, comprising the steps of: collecting data from scanning the circuits of said semiconductor chip having LSSD diagnostic registers on chip for a failing cell for desired handing of multiple failures on a failing chip for immediate scan-out off-chip at a level of assembly test after scan initialization of the LSSD diagnostic registers on the semiconductor chip, said level of assembly test being selected from any level of a group consisting of: an initial manufacturing wafer test, a module test, a system level test, regardless of the clocking methodology, and for the desired failing chip handling on chip of multiple bit failure detection; providing data collection of a first failing cell in said LSSD diagnostic registers, and then skipping the collection of data up to a programmed amount to skip up to a subsequent failing cell, and recording the failure of a next failing cell recognized after said subsequent failing cell in said LSSD diagnostic registers while making reuse of logic including existing address registers for providing data synchronous with fail determination circuits for data collection used for collection of data of said first failing cell, and then pinpointing an actual failure for said next failing cell using additional data collected by reuse of the logic for data collection used for collection of data of said first failing cell. The foregoing limitations are not found in the prior arts of record. The prior art of record, namely Yasui, teaches a method of analyzing a repair of failure memory cell in a memory, which is capable of searching a must-repair of a memory at high speed and of performing a simulation process for relieving a must-repair at high speed at the time point when it has been detected.

There are provided a row address failure number counter/memory for counting the number of failure memory cells on each row address in the row address direction and storing it and a column address failure number counter/memory for counting the number of failure memory cells on each column address in the column address direction and storing it. The stored value in either one counter/memory is read out and the number of failure memory cells on each address is compared with the number of spare lines. The state that the number of failure memory cells on each address is greater than the number of spare lines is determined to be a must-repair, and a simulation process for relieving the failure is executed at the time point when the must-repair has been detected. Furthermore, Yasui teaches (Figure 5) a block diagram showing a schematic configuration of memory testing apparatus having failure relief analyzer. This memory testing apparatus TES comprises a main controller 111, a pattern generator 112, a timing generator 113, a waveform formatter 114, a logical comparator 115, a driver 116, an analog level comparator 117, a failure analysis memory 118, a failure relief analyzer 120, a logical amplitude reference voltage source 121, a comparison reference voltage source 122 and a device power source 123. The main controller 111 is generally constituted by a computer system in which a test program PM created by a user (programmer) is loaded in advance, and the control of the entire memory testing apparatus is performed in accordance with the test program PM. This main controller 111 is connected, via a tester bus BUS, to the pattern generator 112, the timing generator 113, the failure analysis memory 118, the failure relief analyzer 120 and the like. The logical amplitude reference voltage source 121, the comparison reference voltage source 122 and the device power source 123 are also connected to the main controller 111. Yasui teaches that before starting the test of the IC memory, various kinds of data are set by the main controller 111. After the various

kinds of data have been set, the test of the IC memory is started. When the main controller 111 issues a test starting command to the pattern generator 112, the pattern generator 112 starts to generate a pattern. The pattern generator 112 supplies a test pattern data to the waveform formatter 114 in accordance with the test program PM. On the other hand, the timing generator 113 generates a timing signal (clock pulses) for controlling operation timings of the waveform formatter 114, the logical comparator 115 and the like. None of the prior arts of record teach nor fairly suggest all the limitations in the independent claim 1 of the present application. In particular, the limitations of "...an initial manufacturing wafer test, a module test, a system level test, regardless of the clocking methodology, and for the desired failing chip handling on chip of multiple bit failure detection; providing data collection of a first failing cell in said LSSD diagnostic registers, and then skipping the collection of data up to a programmed amount to skip up to a subsequent failing cell, and recording the failure of a next failing cell recognized after said subsequent failing cell in said LSSD diagnostic registers while making reuse of logic including existing address registers for providing data synchronous with fail determination circuits for data collection used for collection of data of said first failing cell, and then pinpointing an actual failure for said next failing cell using additional data collected by reuse of the logic for data collection used for collection of data of said first failing cell..." are not taught nor fairly suggested in the prior arts of record.

Dependent claims 2-7 depend from independent claim 1 and inherently include limitations therein and therefore are allowed as well.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 571-272-3817. The examiner may normally be reached Mon – Thur 6:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 571-272-3819.

Mujtaba Chaudry
Art Unit 2133
March 2, 2006

ALBERT DECADY
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